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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,681	02/25/2002	Naoki Yada	XA-9627	4689

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
HO, THANG H	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,681	YADA ET AL.	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *June 29, 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated June 29, 2004. The applicant's remarks and amendment were considered with the results that follow.

2. Claims 1-44 are pending in this application for examination. Claims 1-3, 5-7, 9, 11-12, 18-19, 25-26, 31-44 have been amended, no claim has been cancelled and no new claim has been added. Therefore, claims 1-44 remain pending in the application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 and 9-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsubara et al. (United States Patent 5,581,503), hereinafter Matsubara.

As per claim 1, Matsubara discloses a microcomputer comprising: an erasable and programmable non-volatile memory **[FIG. 1, FLASH MEMORY FMRY]**; and a CPU **[FIG. 1, CPU]**, wherein the CPU is capable of temporarily branching to a process corresponding to information in a programmable first register means **[FIG. 18, PROGRAM/ERASE CONTROL REGISTER]** for each cycle of a unit process for the non-volatile memory, the unit process including the application of an erase voltage for an erase operation or a program voltage for a programming operation, and a verify operation

[in order to confirm the write state, the central processing unit CPU issues a write cycle to the control register CREG and sets a program verify bit PV (step S6) (FIG. 21, S6, column 27, lines 18-20].

As per claim 2, Matsubara discloses that the CPU skips the branch process when the information in the first register means is a first set value, and branches to the process when the information is other than the first set value **[The central processing unit CPU checks coincidence of read-out data with data utilized for write (step S7). If the central processing unit CPU confirms coincidence through verify, it clears to program verify bit PV (step S8), thus completing write of the one-byte data. On the other hand, if the central processing unit CPU confirms non-coincidence through verify by step S7, it clears the program verify bit PV in step S9 (FIG. 21, S7-S9, column 27, lines 27-41)]**.

As per claims 3 and 40, Matsubara discloses the microcomputer, further including second register means (FKEY) **[counter]** readable and writable by the CPU, and wherein the non-volatile memory sets a second set value in the second register means as a necessary condition for enabling erase and programming operations **[In the initial step of data write in a unit of byte, the central processing unit CPU sets one to a counter n built therein (step S1) (FIG. 21, column 27, lines 1-3)... Upon erase, the central processing unit CPU sets one to its built-in counter n (step S21) (FIG. 23, column 27, lines 49-50)]**, and the CPU sets a value other than the second set value in the

second register means upon the branch and resets the second set value in the second register means for each return from the branch **[If the write retry upper-limit frequency N is not reached, the central processing unit CPU increments the value of counter n by one (step S11) and repeats the processing beginning with the step S3 (FIG. 21, column 27, lines 38-41)... If the final address is not reached, the central processing unit CPU increments the verify address-by one (step S33) and repeats the processing beginning with the step S29 (FIG. 23, column 28, lines 31-34)]**.

As per claims 4 and 41, Matsubara discloses that the value other than the second set value is code information indicative of the progress of an erase and program process **[if the central processing unit CPU confirms non-coincidence through verify by step S7, it clears the program verify bit PV in step S9 and thereafter decides whether the value of counter n reaches a write retry upper-limit frequency N (step S10). Thus, if the write retry upper-limit frequency N is reached, defective write is determined and the processing ends (column 27, lines 32-38)]**.

As per claims 5 and 42-43, Matsubara discloses the microcomputer, further including an interrupt control circuit **[INTERRUPTION CONTROLLER IRCONT]** that inputs an interrupt request signal therein, and performs arbitration of interrupt requests which compete with one another, and an interrupt priority level-based interrupt mask process to thereby output an interrupt signal to the CPU, and wherein the CPU causes the interrupt control circuit to carry out a setting for masking an interrupt lower in

interrupt priority level than a non-maskable interrupt **[NMI designates a non-maskable interrupt signal for applying a non-maskable interruption to the interruption controller ICONT. Other interruption signals, not shown, are applied to the interruption controller ICONT through the ports PORT8 and PORT9 (FIG. 14, column 22, lines 27-44)][when the second operation mode is set in the microcomputer MCU, the ports PORT2 to PORT5 and PORT8 are allotted, though not limitedly, for connection to the PROM writer adapted to control write of the flash memory FMRY. More specifically, the port PORT2 is allotted for input/output of data EDO to ED7 for write and verify and the ports PORT3 to PORT5 and PORT8 are allotted for input of address signals EA0 to EA16 as well as input of access control signal CE* (chip enable signal), OE* (output enable signal) and WE* (write enable signal). The chip enable signal CE* is an operation selection signal for the flash memory FMRY delivered from the PROM writer, the output enable signal OE* is a designation signal of an output operation for the flash memory FMRY and the write enable signal WE* is a designation signal of a write operation for the flash memory FMRY. For inputting one-bit EA9 of address signals EA0 to EA16, the input terminal of the signal NMI is allotted. External terminals of the thus allotted ports and other necessary external terminals including the application terminal of high voltage Vpp are connected to the general purpose PROM writer through the conversion socket SOCKET explained in connection with FIG. 3. Conveniently, the allotment of the external terminals at that time can be done in the form of such a terminal arrangement that the microcomputer MCU can**

be connected with ease to the PROM writer PRW through the conversion socket SOCKET. The external terminals allotted for connection to the PROM writer PRW in the second operation mode are assigned with other functions in the other operation mode of the microcomputer MCU (column 22, line 60 through column 23, line 23)].

As per claim 6, Matsubara discloses that the CPU executes a process that changes a location of an interrupt process routine for a non-maskable interrupt request to an address of a RAM upon execution of the erase and programming **[When the first operation mode is designated, the central processing unit CPU executes the transfer control program to transfer the rewrite control program to the random access memory RAM. After completion of the transfer, the processing of the central processing unit CPU branches to execution of the rewrite control program on the random access memory RAM and through this, the erase and write (inclusive of verification) of the flash memory FMRY is repeated (column 13, lines 36-48)]**.

As per claim 7, Matsubara discloses a microcomputer comprising: an erasable and programmable non-volatile memory **[FIG. 1, FLASH MEMORY FMRY]**; and a CPU **[FIG. 1, CPU]**, wherein the non-volatile memory has an erase and program control program executed by the CPU and used for erase/program-controlling of non-volatile memory, wherein the erase and program control program allows a process of the CPU to temporarily branch to another process for each cycle of a unit process for the non-volatile

memory, the unit process including the application of an erase voltage for an erase operation or a program voltage for a programming operation and a verify operation, and wherein the CPU specifies the another process according to a value set in a first register means **[FIG. 1, MODE] [a rewrite control program and a transfer control program have precedently been written in predetermined areas of the flash memory. When the first operation mode is designated, the central processing unit CPU executes the transfer control program to transfer the rewrite control program to the random access memory RAM and through this, the erase and write (inclusive of verification) of the flash memory FMRY is repeated (column 13, lines 36-48)]**.

As per claims 9 and 44, Matsubara discloses the microcomputer, further including a RAM **[FIG. 3 - FIG. 5, RAM]** disposed in an address space of the CPU, and wherein the non-volatile memory has a transfer control program that transfers the erase and program control program to the RAM, and the CPU sets parameters for the another process to the erase and program control program transferred to the RAM, based on the set value of the first register means and thereby executes the erase and program control program **[a rewrite control program and a transfer control program have precedently been written in predetermined areas of the flash memory. When the first operation mode is designated, the central processing unit CPU executes the transfer control program to transfer the rewrite control program to the random access memory RAM and through this, the erase and write (inclusive of verification) of the flash memory FMRY is repeated (FIG. 5, column 13, lines 36-48)]**.

As per claims 10-16, the claims encompass the same scope of invention as to that of claims 1-4 and 7-9. The claims are therefore rejected for the same reasons as set forth above with respect to claims 1-4 and 7-9. In addition, Matsubara discloses that when information is written into the specified memory cell of the electrically programmable plural memory cells, the program control program defines a process for executing a plurality of times of program process loops and writing the corresponding information into the specified memory cell, and wherein the process of the central processing unit is capable of branching to the first control program for the each program process loop **[see FIG. 21]**; and that each of the plurality of memory cells is an electrically programmable and erasable non-volatile memory cell having a floating gate/electrically programmable and erasable flash memory **[Abstract, FIG. 1 and column 1; lines 11-14].**

As per claims 17-23, the claims encompass the same scope of invention as that of claims 10-16. The claims are therefore rejected for the same reasons set forth above with respect to claims 10-16 **[Noting that Matsubara discloses a microcomputer for erasing, programming, and verifying of a flash memory device, thus it is inherent that the CPU is capable of branching to any parts of the control programs depending on the mode operation set within the MODE register]**.

As per claims 24-33, the claims encompass the same scope of invention as that of claims 10-16 and 17-23. The claims are therefore rejected for the same reasons set forth above with respect to claims 10-16 and 17-23.

As per claims 34 and 36-37, Matsubara discloses a programming method that causes a central processing unit included in a microcomputer having the central processing unit **[FIG. 1, CPU]** and an electrically programmable non-volatile memory **[FIG. 1, FLASH MEMORY FMRY]** to execute a program control program to thereby write information into the non-volatile memory, comprising: a first step of supplying an address for a memory cell to be programmed in the non-volatile memory **[CPU performs the memory write operation explained in connection with FIG. 20 to set data to be written in the flash memory FMRY to the data input latch circuit DILAT shown in FIG. 16 and set and address to be written with the data to the address latch circuit ALAT (step S2) (FIG. 20, FIG. 21, S2 and column 27, lines 1-8)]**; a second step of supplying information to be programmed to the memory cell **[CPU performs the memory write operation explained in connection with FIG. 20 to set data to be written in the flash memory FMRY to the data input latch circuit DILAT shown in FIG. 16 and set and address to be written with the data to the address latch circuit ALAT (step S2) (FIG. 20, FIG. 21, S2 and column 27, lines 1-8)]**; and a third step of repeatedly performing a writing operation to write information into the memory cell, the writing operation including: a voltage applying step of applying a program voltage to the memory cell **[the control circuit FCONT applies, on the basis of the data and address**

set in the step S2, high voltages to the control gate and the drain of a memory cell designated by the address to perform write (FIG. 21, S3, column 27, lines 1-41]; a verify step of confirming whether the information to be programmed has been written into the memory cell **[in order to confirm the write state, the central processing unit CPU issues a write cycle to the control register CREG and sets a program verify bit PV (step S6) (FIG. 21, S6, column 27, lines 18-20]**; a step of referring to a value of a predetermined register and transitioning a process of the central processing unit during execution of the third step to a predetermined process corresponding to a predetermined value set to the register when the predetermined value is stored in the register **[The central processing unit CPU checks coincidence of read-out data with data utilized for write (step S7). If the central processing unit CPU confirms coincidence through verify, it clears to program verify bit PV (step S8), thus completing write of the one-byte data. On the other hand, if the central processing unit CPU confirms non-coincidence through verify by step S7, it clears the program verify bit PV in step S9 (FIG. 21, S7-S9, column 27, lines 27-41)]**; and a step of returning the process of the central processing unit from the predetermined process to the third step **[If the write retry upper-limit frequency N is not reached, the central processing unit CPU increments the value of counter n by one (step 11) and repeats the processing beginning with the step S3 (FIG. 21, S11, column 27, lines 38-41)]**. In addition, Matsubara discloses the step for causing the process of the central processing unit to transit to the predetermined process includes a step for referring to a value of a predetermined register and allowing the process thereof to transit to the predetermined

process corresponding to the value set to the register where the predetermined value is stored in the register **[column 27, lines 36-41]**.

As per claims 35 and 38-39, the claims encompass the same scope of invention as that of claims 34 and 36-37. The claims are therefore rejected for the same reasons set forth above with respect to claim 34 and 36-37. In addition, Matsubara clearly discloses the erasing method comprising the required steps in FIG. 22, column 27, lines 42-52.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsubara et al. (United States Patent 5,581,503), hereinafter Matsubara.

As per claim 8, Matsubara teaches the invention substantially as claimed. Although Matsubara does not teach expressly that the first register means is a register selected from general purpose registers of the CPU, Matsubara teaches that a register means, i.e. the second register means, can be selected from the general purpose registers of the CPU **[column 27, lines 1-3]**. Accordingly, it would have been prima facie obvious for one skilled in the art at the time the invention was made to implement the first register means utilizing a general purpose registers of the CPU as taught by Matsubara to

generate the claimed invention with a reasonable expectation of success. One skilled in the art would have been motivated to do so, because it would provide space savings and improve access time, thereby reducing costs and increasing system performance of the overall system.

Response to Arguments

7. Applicant's arguments with respect to claims 1-44 have been fully considered but they are not persuasive.

Applicants asserted that Matsubara fails to teach or suggest the "branching to a process corresponding to information in a programmable first register means for each cycle". Examiner respectfully traverses Applicant's remarks. Matsubara clearly teaches that a rewrite control program and a transfer control are written to the predetermined areas of the flash memory corresponding to the first register means. When the first operation mode is designated, the central processing unit CPU executes the transfer control program to transfer (i.e., branch) the rewrite control program to the random access memory RAM and through this, the erase and write (inclusive of verification) of the flash memory FMRY is repeated (FIG. 5, column 13, lines 36-48)]. Therefore, the rejection of claims 1-44 is deemed to be proper.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 571-272-4206. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan
10/18/04

Thang Ho
Art Unit 2188
October 18, 2004

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER